ABSTRACT

An analog multiplier for multiplying a first analog voltage signal at a first frequency by a second analog voltage signal at a second frequency, comprising a first stage for converting the first analog voltage signal into a first and a second current signals, and a second stage comprising a first and a second cross-coupled current-switching pairs, driven by the second voltage signal, the first and second current-switching pairs having respective current inputs for receiving the first and the second current signals, respectively. Parasitic capacitances are inherently associated with each current input of the current-switching pairs. A compensation circuit is coupled to the current inputs of the current-switching pairs for compensating the parasitic capacitances.